



PROFILE

An aspiring, highly motivated professional having masters in Electrical Engineering (System-on-Chip). Possess a sound background in microelectronics, analog, digital and mixed-signal IC design, simulations and layout. Experienced in testing and validation. Well versed in research and technical report writing. Currently looking for challenging PhD position to leverage expertise and acquire new skills over time towards a positive career growth.

CONTACT

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HOBBIES

Reading
Spirituality
IC die photo collection

MUHAMMAD UMER KHALID

Manager Microelectronics Testing

EDUCATION

MSc Electrical Engineering Linkoping University Sweden

Aug 2009 – Aug 2012

System on Chip Design. 6 bit DAC tape out in AMS 0.35 um

Master's thesis: Multilevel Embedded DRAM 90 nm, EPFL Switzerland

BSc Electrical Engineering University of Azad Jammu Kashmir Pakistan

Aug 2004 – Aug 2008

Specialization: Electronics/Telecom, CGPA: 3.64/4

WORK EXPERIENCE

Institute of Applied Technologies Manager Microelectronics Testing

April 2017–Present

Testing of Thermal Imaging Systems, Focal Plane Arrays

Room and Cryogenic Testing of Readout Integrated Circuits

Test setup development

Institute of Applied Technologies IC Designer

Aug 213–April 2017

Analog and Mixed Signal IC Design

Two stage OTA, Analysis of pixel preamplifiers, Std cell layout

60% of layout for tapeout of 640x512 image sensor ROIC in 0.35 um

University of Poonch Rawalakot Lecturer

Nov 2012–Aug 2013

Volunteered in establishment of Electrical Engineering Department

Development of labs and library, entry test, teaching circuit theory

SKILLS

Analog and mixed signal IC design

Testing of ICs and thermal imaging systems

Cadence Virtuoso, Spectre, Encounter, Synopsys Design Compiler

Altium Designer, LabVIEW, MATLAB, Cypress PSoC Creator

Multilayer PCB design

Verilog HDL, VHDL, System C, C++

Team and project management